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10/606,462	06/26/2003	Scott L. Michaelis	200205355-1	3496

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EXAMINER	
SUGENT, JAMES F	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 06/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/606,462	MICHAELIS ET AL.	
	Examiner	Art Unit	
	James Sugent	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2003 and 22 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☒ Claim(s) *14 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *March 26, 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is sent in response to Applicant's Communication received March 29, 2006 for application number 10/606462 originally filed June 26, 2003.

It is hereby acknowledged the following papers have been received: amendment to the specification for minor typographical error in paragraph 23; annotated drawing of drawing number 3 of 4; and, corrections made to minor claims 14 and 22.

Claim Objections

Claims 14 and 22 are objected to because of the following informalities:

- Both claim 14 and 22 contain the use of the trademark/trade name INTEL cited as "IA-64" (standing for Intel Architecture-64: see http://en.wikipedia.org/wiki/IA-64) as a limitation to identify or describe a particular material or product. The claim scope is uncertain since the trademark or trade name cannot be used properly to identify any particular material or product. A trademark or trade name is used to identify a source of goods, and not the goods themselves. Thus, a trademark or trade name does not identify or describe the goods associated with the trademark or trade name. Therefore, the claim is rendered indefinite.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harrington et al. (U.S. Patent Publication No. 2003/0236972 A1) (hereinafter referred to as Harrington) in view of Forsman et al. (U.S. Patent No. 6,742,139) (hereinafter referred to as Forsman), Okuyama (U.S. Patent Publication No. 2002/0116469) (hereinafter referred to as Okuyama) and Dawkins et al. (U.S. Patent No. 6,820,207 B2) (hereinafter referred to as Dawkins).

As to claim 1, Harrington discloses a method for resetting a partition of a multiple partition system, wherein the partition (230) comprises a plurality of processors (232, 234, 236, 238 and 290), the method comprising: executing, by one processor of the plurality of processors (290), reset code from firmware (hypervisor 210) (Dawkins discloses the partition 230 being reset by the service processor 290; paragraph 41 and paragraph 42, lines 1-6 and paragraph 51, lines 1-4).

Harrington fails to disclose resetting the one processor by writing to its associated reset register, sending an interrupt to the other processors of the plurality of processors and resetting the other processors by writing a reset code to their associated reset registers.

Forsman teaches a multiprocessor system (figure 1) wherein the service processor (135) itself or a host will set a bit within the service processor's status/control register (reset register) to cause an interrupt thus causing a reset if failure is detected (column 3, lines 51-55 and column 4,

lines 46-50). Forsman has the additional feature of monitoring a heartbeat signal of the service processor to determine a failure in the service processor (column 1, lines 31-38).

It would have been obvious to one of ordinary skill of the art having the teachings of Harrington and Forsman at the time the invention was made, to modify the partition reset process of Harrington to include having an interrupt sent to the service processor to reset the processor by setting a bit within it's status/control register (reset register) as taught by Forsman such that the one processor that reset all of the other partition processors is interrupted and reset by writing to its associated reset register in addition to resetting and sending an interrupt to the other processors by writing a reset code to their associated reset registers. One of ordinary skill in the art would be motivated to make this combination of resetting the service processor by setting a bit in it's reset register in view of the teachings of Forsman, as doing so would give the added benefit of monitoring a heartbeat signal of the service processor to determine a failure in the service processor (column 1, lines 31-38).

Neither Harrington nor Forsman disclose building a list of reset register addresses associated with the plurality of processors.

Dawkins teaches a multiprocessor partition wherein the service processor (366) in cooperation with NVRAM (368) creates (build) objects (table set stored in NVRAM which is inclusive of addresses; column 10, lines 16-18) that consists of profiles used to configure and manage processors (301, 302, 303, 304) within the logical partition (column 5, line 63 thru column 6, line 6). Dawkins also discloses sending an interrupt to the other processors of the plurality of processors (column 10, line 65 thru column 11, line 5). Dawkins further discloses resetting (activating) the other processors by activating the system reset signals in all of the

processors (proper register location as is known in the art) (column 10, lines 8-21). Dawkins has the added feature of controlling power within a logical processor (column 2, lines 2-5).

It would have been obvious to one of ordinary skill of the art having the teachings of Harrington, Forsman and Dawkins at the time the invention was made, to modify the partition management process of Harrington to include creating profiles of all of the processors within the partition that contain addresses as taught by Dawkins such that each processor's profile would include the address of the reset register. One of ordinary skill in the art would be motivated to make this combination of building and maintaining processor profiles in view of the teachings of Dawkins, as doing so would give the added benefit of controlling power within a logical processor (column 2, lines 2-5).

As to claim 2, Forsman teaches the method further comprising: storing the firmware on a read only memory (paragraph 42).

As to claim 3, Dawkins teaches the method further comprising: storing the list of reset register addresses in random access memory (NVRAM; column 5, line 63 thru column 6, line 5).

As to claim 4, Harrington disclose the method wherein the last reset register address on the list (as discussed hereinabove) is a reset register address for the cell that is executing the reset code (Harrington discloses the service processor resetting all of the partition processors and then resetting itself which necessitates the last processor on the list is the service processor; paragraph 51, lines 4-8).

As to claim 5, Harrington discloses the method further comprising: requesting the execution of the reset code by a processor (service processor) of the plurality of processors (paragraph 51, lines 1-4).

As to claim 6, Harrington discloses the method further comprising: requesting the execution of the reset code by an operating system of the multiple partition system (paragraph 9).

As to claim 7, Harrington discloses the method further comprising: requesting the execution of the reset code by a firmware shell (hypervisor) of the multiple partition system (paragraph 51).

As to claim 8, Harrington discloses the method wherein building the list comprises: writing the address of the one processor (service processor) last in the list (Harrington discloses the service processor resetting all of the partition processors and then resetting itself which necessitates the last processor on the list is the service processor; paragraph 51, lines 4-8).

As to claim 9, Forsman teaches the method further comprising: flushing a cache associated with the one processor, after sending the interrupt (column 3, lines 39-47).

As to claim 10, Harrington discloses the method further comprising: moving execution from main memory to read only memory (paragraph 51).

As to claim 11, Dawkins teaches the method further comprising: switching from virtual memory mode into physical memory mode (column 6, line 66 thru column 7, line 27).

As to claim 12, Dawkins teaches the method wherein the partition comprises a plurality of cells, and each cell comprises at least one processor, the method further comprises: inventorying the plurality of cells for resetting (managing processor profiles; column 5, line 63 thru column 6, line 5).

As to claim 13, Forsman teaches the method wherein resetting the one processor occurs after resetting the other processors (as discussed hereinabove in claim 1).

As to claim 14, Dawkins teaches the method wherein the plurality of processors are IA-64 processors, and the firmware is system abstraction layer firmware (column 6, line 66 thru column 7, line 27).

Claims 15-16 and 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harrington et al. (U.S. Patent Publication No. 2003/0236972 A1) (hereinafter referred to as Harrington) in view of Dawkins et al. (U.S. Patent No. 6,820,207 B2) (hereinafter referred to as Dawkins).

As to claim 15, Harrington discloses a partition of multiple partition computer system comprising: a plurality of processors (232, 234, 236, 238 and 290); firmware (hypervisor 210) comprising reset code that resets a portion of the partition (paragraph 40, lines 3-6 and paragraph 42, lines 1-6), wherein one processor (366) of the plurality of processors executes the reset code (paragraph 51, lines 1-8); and, random access memory (NVRAM 192).

Harrington fails to disclose that the random access memory is not affected by the reset code that stores a list of addresses associated with the portion.

Dawkins teaches a multiprocessor partition wherein the service processor (366) in cooperation with NVRAM (368) creates (build) objects (plural of object and therefore list) that consists of profiles used to configure and manage processors (301, 302, 303, 304) within the logical partition (column 5, line 63 thru column 6, line 6). Dawkins has the added feature of controlling power within a logical processor (column 2, lines 2-5).

It would have been obvious to one of ordinary skill of the art having the teachings of Harrington and Dawkins at the time the invention was made, to modify the partition management process of Harrington to include creating profiles of all of the processors within the partition that

contain addresses as taught by Dawkins such that each processor's profile would include the address of the reset register. One of ordinary skill in the art would be motivated to make this combination of building and maintaining processor profiles in view of the teachings of Dawkins, as doing so would give the added benefit of controlling power within a logical processor (column 2, lines 2-5).

As to claim 16, Dawkins teaches the partition further comprising: read only memory that stores the firmware (column 6, lines 36-45).

As to claim 21, Dawkins discloses the partition wherein the one processor is reset after the other processors of the plurality of processors are reset.

As to claim 22, Dawkins discloses the partition wherein the plurality of processors are IA-64 processors, and the firmware is system abstraction layer firmware.

Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dawkins et al. (U.S. Patent No. 6,820,207 B2) (hereinafter referred to as Dawkins) in view of Forsman et al. (U.S. Patent No. 6,742,139) (hereinafter referred to as Forsman).

As to claim 23, Dawkins discloses a computer readable medium having computer program logic recorded thereon for operating a partition of a multiple partition computer system, wherein the partition comprises a plurality of processors (432, 434, 436, 438), the computer program logic comprising: means for (hypervisor 410 and service processor 366) building a list of addresses (table set stored in NVRAM which is inclusive of addresses; column 10, lines 16-18) associated with the plurality of processors (Dawkins discloses the firmware hypervisor 410 performs a number of functions and services for the operating systems to create and enforce the partitioning of logically partitioned platform which would include creating profiles of all of the

processors within a partition which, as is known in the art, may include addresses associated with the partition; column 5, lines 63 thru column 6, line 6 and column 6, lines 36-39); means for (service processor 366) placing each processor of the plurality of processors into a known state (Dawkins discloses the service processor placing the partition processors into a power off state; column 10, lines 30-34); means for (service processor 366) resetting the plurality of processors (column 10, lines).

Dawkins fails to disclose writing a reset code into the plurality of processor's associated reset registers.

Forsman teaches a multiprocessor system (figure 1) wherein the service processor (135) itself or a host will set a bit within the service processor's status/control register (reset register) to cause an interrupt thus causing a reset if failure is detected (column 3, lines 51-55 and column 4, lines 46-50). Forsman has the additional feature of monitoring a heartbeat signal of the service processor to determine a failure in the service processor (column 1, lines 31-38).

It would have been obvious to one of ordinary skill of the art having the teachings of Dawkins and Forsman at the time the invention was made, to modify the partition reset process of Dawkins to include a processor being reset by setting a bit within it's status/control register (reset register) as taught by Forsman such that resetting the processors within the partition by writing a reset code to their associated reset registers. One of ordinary skill in the art would be motivated to make this combination of resetting a processor by setting a bit in it's reset register in view of the teachings of Forsman, as doing so would give the added benefit of monitoring a heartbeat signal of the service processor to determine a failure in the service processor (column 1, lines 31-38).

Claims 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harrington et al. (U.S. Patent Publication No. 2003/0236972 A1) (hereinafter referred to as Harrington) and Dawkins et al. (U.S. Patent No. 6,820,207 B2) (hereinafter referred to as Dawkins) as applied to claim 15 above, and further in view of Forsman et al. (U.S. Patent No. 6,742,139) (hereinafter referred to as Forsman).

As to claim 17, Dawkins teaches the partition further comprising: a plurality of cells (232, 234, 236, 238); wherein each cell comprises at least one processor (one processor per cell) of the plurality of processors, and each cell comprises an address that is on the list (table set with addresses; column 5, line 63 thru column 6, line 5 and column 10, lines 16-18).

Neither Harrington nor Dawkins teach the addresses on the list are the addresses to reset registers.

Forsman teaches a multiprocessor system (figure 1) wherein the service processor (135) itself or a host will set a bit within the service processor's status/control register (reset register) to cause an interrupt thus causing a reset if failure is detected (column 3, lines 51-55 and column 4, lines 46-50). Forsman has the additional feature of monitoring a heartbeat signal of the service processor to determine a failure in the service processor (column 1, lines 31-38).

It would have been obvious to one of ordinary skill of the art having the teachings of Harrington, Dawkins and Forsman at the time the invention was made, to modify the address profile data for each processor in the partition management process of Harrington to include the address of the status/control register (reset register) as taught by Forsman such the addresses stored in the processor profile table set were the addresses to the reset registers. One of ordinary skill in the art would be motivated to make this combination of using the status/control register

(reset register) in view of the teachings of Forsman, as doing so would give the added benefit of monitoring a heartbeat signal of the service processor to determine a failure in the service processor (column 1, lines 31-38).

As to claim 18, Forsman teaches the partition wherein each cell is reset by writing a reset code (as discussed hereinabove) to its associated reset register (column 4, lines 46-50).

As to claim 19, Dawkins teaches the partition wherein the address on the list is a reset register address for the cell that comprises the one processor (as discussed hereinabove in claim 17).

As to claim 20, Harrington discloses the partition wherein each cell further comprises resources other than the at least one processor, and a portion of the resources is reset when the cell is reset (paragraph 51, lines 9-11).

Response to Arguments

Applicant's arguments with respect to claims 1-23 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Sugent whose telephone number is (571) 272-5726. The examiner can normally be reached on 8AM - 4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at (866) 217-9197 (toll-free).

James Sugent
Patent Examiner, Art Unit 2116
May 23, 2006

THUAN N. DU
PRIMARY EXAMINER